NCN5193NGEVB

NCN5193NG Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Introduction

The NCN5193NGEVB includes all external components needed for operating NCN5193 and demonstrates the small PCB surface area such an implementation requires. The EVB allows easy design of HART implementations using NCN5193.

Overview

The NCN5193 is a single-chip, CMOS modem for use in highway addressable remote transducer (HART) field instruments and masters. The modem and a few external passive components provide all of the functions needed to satisfy HART physical layer requirements including modulation, demodulation, receive filtering, carrier detect, and transmit-signal shaping.

The NCN5193 also includes an internal 17-bit sigma-delta modulation DAC for easy implementation of slave devices. An SPI bus provides easy communication to this DAC and internal registers.

Features

- Single-chip, Half-duplex 1200 bits per Second FSK Modem
- Bell 202 Shift Frequencies of 1200 Hz and 2200 Hz
- 1.8 V − 3.5 V Power Supply
- Transmit-signal Wave Shaping
- Receive Band-pass Filter
- Low Power: Optimal for Intrinsically Safe Applications
- Compatible with 1.8 V or 3.5 V Microcontroller
- Internal Oscillator with 3.68 MHz Crystal
- Meets HART Physical Layer Requirements
- Includes 17-bit DAC for Slave Implementation
- Industrial Temperature Range of −40°C to +85°C
- Available in 32-pin QFN

Applications

- HART Multiplexers
- HART Modem Interfaces
- 4-20 mA Loop Powered Transmitters

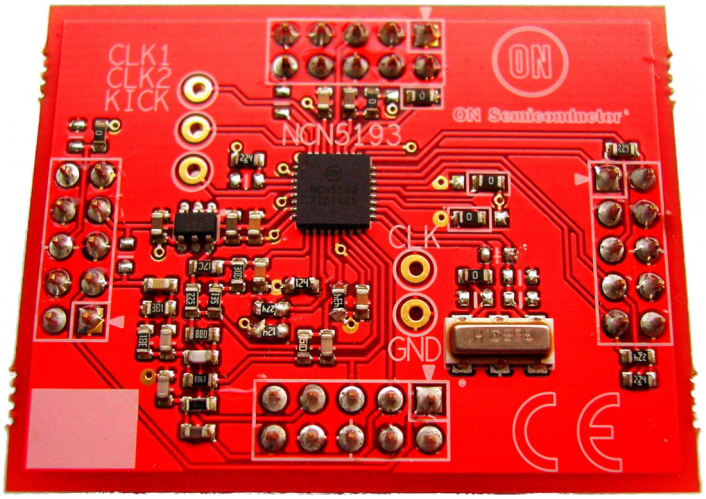

Figure 1. NCN5193NGEVB Evaluation Board

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Table 1. ELECTRICAL CHARACTERISTICS OF THE NCN5193NGEVB BOARD

Symbol	Characteristic	Min	Typ	Max	Units
V_{DD}	Supply Voltage	1.80	3.00	3.50	V
Current Consumption					
I_{DD}	V_{DD} = 1.80 V, idle	−	170	−	μA
I_{DD}	V_{DD} = 3.00 V, idle	−	215	−	μA
I_{DD}	V_{DD} = 3.50 V, idle	−	240	−	μA
I_{DD}	External Clock, V_{DD} = 1.80 V, idle	−	130	−	μA
I_{DD}	External Clock, V_{DD} = 3.50 V, idle	−	180	−	μA
Transmitted Frequency					
f_M	Mark “1”	−	1194	−	Hz
f_S	Space “0”	−	2204	−	Hz
Levels					
V_{TxA}	Amplitude Transmit Output	−	500	−	mV p-p
V_{CD}	Carrier Detect Level	−	110	−	mV p-p
Reference Voltages					
V_{AREF}	AREF	−	1.248	−	V
V_{CDREF}	CDREF	−	1.163	−	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NCN5193 Description

The NCN5193 modem is a single-chip CMOS modem for use in HART field instruments and masters. It includes on-chip oscillator and a modulator and demodulator module communicating with a UART without internal buffer, as well as an internal 17 bit sigma delta DAC. The NCN5193 requires some external filter components and a 460.8 kHz, 921.6 kHz, 1.84 MHz or 3.68 MHz clock source. This clock source can either be the interface oscillator by using a crystal or ceramic resonator, or an external clock signal.

When the device is transmitting data, the receive module is shut down and vice versa to conserve power. With simple power-saving maneuvers, the IC can be made to operate with a current consumption of as little as 130 μA. The same techniques apply as explained for the A5191HRT in the Design Note “A5191HRT Design for Low-Power Environments” (AND9030/D).

Test and Measurement Tools

Listed below are the tools used to acquire the values presented in this evaluation board.

- Oscilloscope: Tektronix DPO4101 1 GHz
- Signal Generator: Agilent 33250A

NCN5193NGEVB DESCRIPTION

Schematic Diagram − BOM List

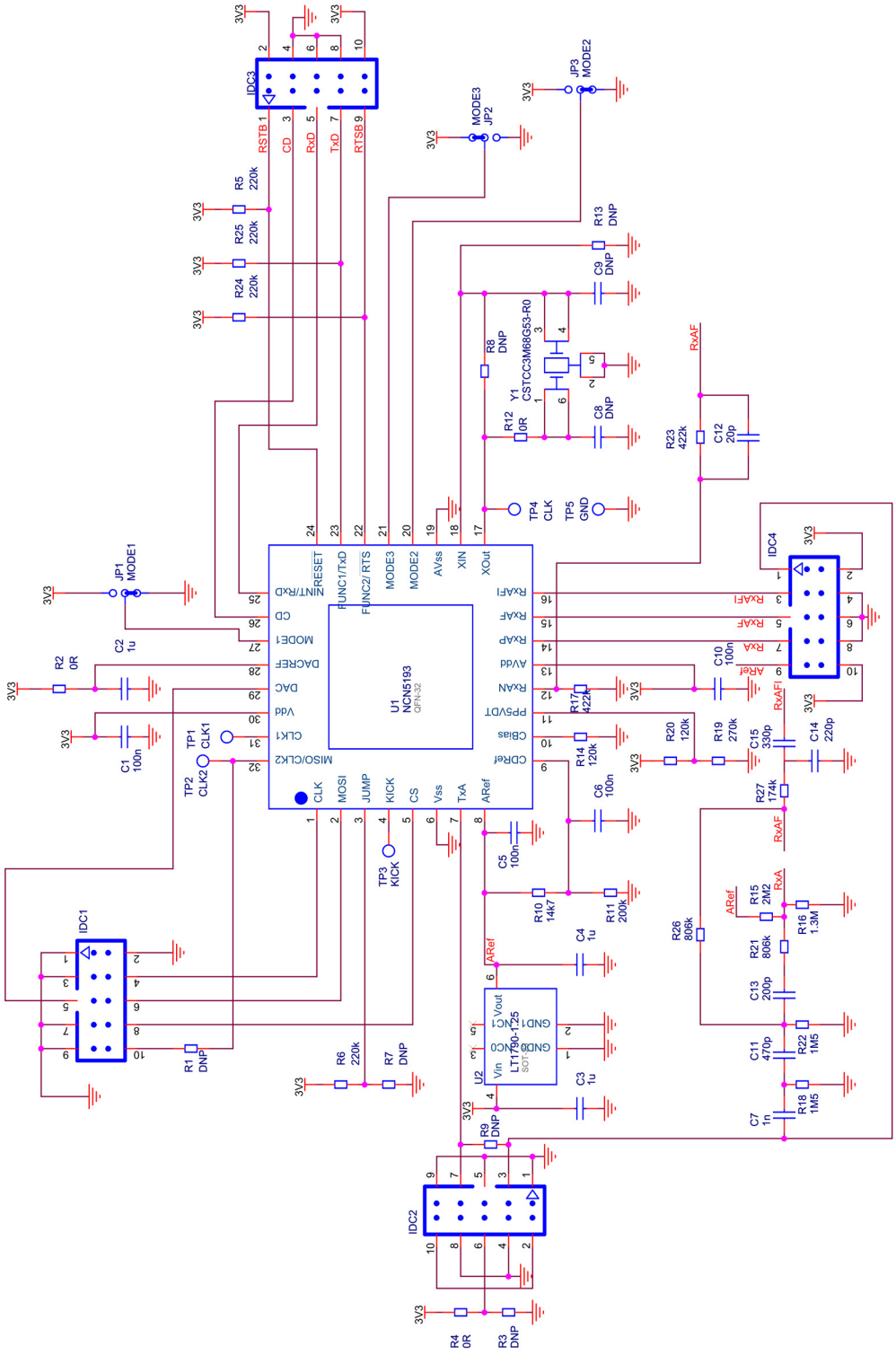

Figure 2. NCN5193NGEVB Schematic

Table 2. NCN5193NGEVB BILL OF MATERIALS

Reference	Manufacturer & Comments	Value	Size	Quantity
C_1, C_5, C_6, C_{10}		100 nF	0603	4
C_2, C_3, C_4		1 μF	0603	3
C_7		1 nF	0603	1
C_8, C_9	Do Not Populate	DNP	0603	2
C_{11}		470 pF	0603	1
C_{12}		20 pF	0603	1
C_{13}		200 pF	0603	1
C_{14}		220 pF	0603	1
C_{15}		330 pF	0603	1
IDC_1, IDC_2, IDC_3, IDC_4		IDC10		4
R_1, R_3, R_7, R_8, R_9, R_{13}	Do Not Populate	DNP	0603	6
R_2, R_4, R_{12}		0 R	0603	3
R_5, R_6, R_{24}, R_{25}		220 kΩ	0603	4
R_{10}		14.7 kΩ	0603	1
R_{11}		200 kΩ	0603	1
R_{14}, R_{20}		120 kΩ	0603	2
R_{15}		2.2 MΩ	0603	1
R_{16}		1.3 MΩ	0603	1
R_{17}, R_{23}		422 kΩ	0603	2
R_{18}, R_{22}		1.5 MΩ	0603	2
R_{19}		270 kΩ	0603	1
R_{21}, R_{26}		806 kΩ	0603	2
R_{27}		174 kΩ	0603	1
TP_1, TP_2, TP_3, TP_4, TP_5	Do Not Populate	DNP		5
U_1	ON Semiconductor	NCN5193		1
U_2	Linear Technology	LT1790−1.25		1
Y_1	Murata	CSTCC3M68G53−R0		1

General Overview

The NCN5193NGEVB evaluation board demonstrates the external components required for the operation of the IC. We will cover the different sections below as well as possible alternatives. A drawing of the board where the different sections are indicated is shown below.

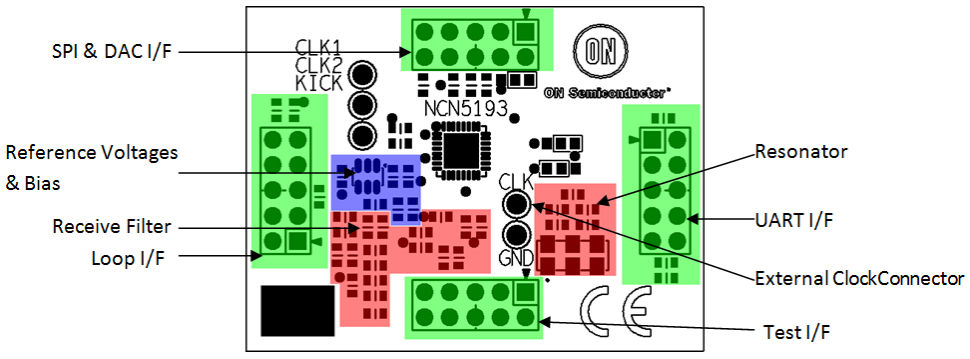

Figure 3. Board Drawing with Indication of Different Sections

Power Supply and References

Power Supply

The NCN5193NGEVB is designed for a nominal voltage of 3 V. However, NCN5193 can be operated with a power supply of 1.8 V to 3.5 V.

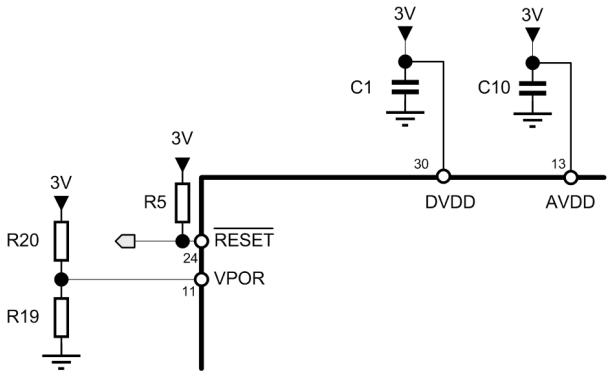

Figure 4. Supply Voltage and Power on Reset

Current consumption of the module is very limited, making it ideal to be battery or loop-powered. Measurements of the power consumption of the module are listed in Table 1.

The module will use less power when clock signal is applied externally, as this allows the modem to shut down the oscillator circuit. As is to be expected, a higher supply voltage increases current consumption.

The NCN5193 includes an internal voltage supervisor. This will guarantee correct operation of the digital circuitry during start-up. All that is required for using this supervisor is an external resistor divider (R_{19}, R_{20}). The voltage supervisor compares the voltage offered by the resistor divider on the VPOR pin to AREF. The resistor divider should be dimensioned such that at the desired turn-on point of the voltage supervisor, the VPOR pin is equal to AREF. On the evaluation board the resistor divider is dimensioned to make the POR trip at 2.8 V.

The voltage supervisor will keep the RESETB pin low until its threshold value is reached, and will then wait an additional minimum of 30 ms until it releases the RESETB. This ensures that some time has passed after the supply voltage reaches the turn-on voltage.

C_1 and C_{10} are 100 nF ceramic decoupling capacitors located directly adjacent to each power pin. For analog power pins, an additional large-value ceramic capacitor may be needed in addition to the 100 nF decoupling capacitor when the application is intended for high-noise environments.

For loop-powered devices, additional decoupling with a large value capacitor is advised to prevent digital noise from being transmitted on the current loop.

Additional ferrite beads in series with power supply lines may help to reduce EMI.

Reference Voltages and Comparator Bias

NCN5193 needs an external analog reference voltage. This reference is used by receiver or demodulator (RX) comparator, carrier detect (CD), and voltage supervisor.

The AREF reference voltage sets the trip point of the demodulation operational amplifier of the NCN5193. The AREF reference voltage is also used in setting the DC operating point of the received signal after it has passed through the band-pass receive filter. The ideal value for the AREF reference voltage depends on the voltage supply, and is chosen roughly half-way the operating range of the operational amplifiers. This ensures the range of the operational amplifier is maximized. A reference voltage of 1.24 V is recommended.

For NCN5193NGEVB, a series regulator is used with an internal reference of 1.25 V. The chosen regulator has a very low supply current, to optimize power usage. Using a series regulator is more desirable from a power usage perspective, as a series regulator's current draw will vary with the output current, whereas a shunt regulator is dimensioned on the maximum current draw and will always draw the same current. Large capacitors on the in- and output of the voltage regulator increase the reference stability.

The CDREF reference voltage sets the threshold for the carrier detect comparator. As the received signal is biased at AREF, the difference between CDREF and AREF will determine the minimum amplitude needed for the carrier detect comparator to flip. A (AREF-CDREF) of 80 mV corresponds to signal of approximately 100 mV peak-to-peak at the input of the receive filter. The CDREF reference voltage on the NCN5193NGEVB is generated by a resistor division of the AREF reference.

An external resistor is required to set the bias current. The voltage over the bias resistor is regulated to AREF, so that the resistor determines a bias current. This bias current controls the operating parameters of the internal operational amplifiers and comparators and should be set to approximately 2.5 μA. For low cost solutions, a 470 kΩ is acceptable with minimal effect on operation.

Table 3. REFERENCE VOLTAGES

Description	Value
AREF Reference Voltage	1.248 V
CDREF Reference Voltage	1.163 V

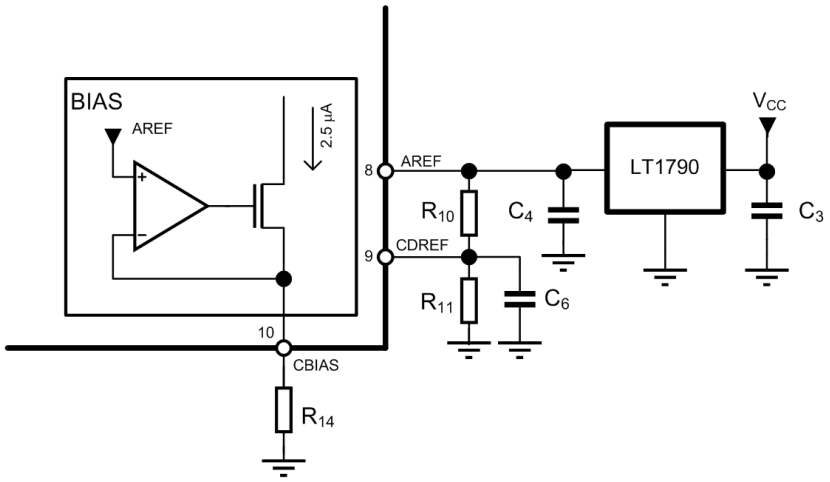

Figure 5. Reference Voltages Schematic

Clock Generation

NCN5193 is operated on a clock signal of either 460.8 kHz, 921.6 kHz, 1.84 MHz or 3.68 MHz. The NCN5193NGEVB has two options for providing this clock signal. The first method is by using a ceramic resonator or a crystal with the internal oscillator. The standard populated option is a Murata CSTCC3M68G53−R0 ceramic resonator, with build-in load capacitors.

Alternatively, a clock signal can be provided externally when R_{12} is removed and R_{13} is populated by a resistor of 0 Ω. This signal can be provided by a microcontroller or any other external oscillator circuit. The module uses less power when clock signal is applied externally, as this allows the modem to shut down the oscillator circuit. A typical current consumption witnessed by utilizing an external oscillator is 60 μA less. However, care must be taken that this external signal has the required frequency accuracy (1%).

Duty cycle of the clock signal is specified between 35% and 65%.

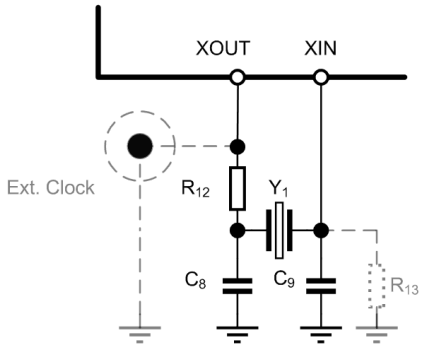

Figure 6. Clock Generation Circuit (Resonator Option)

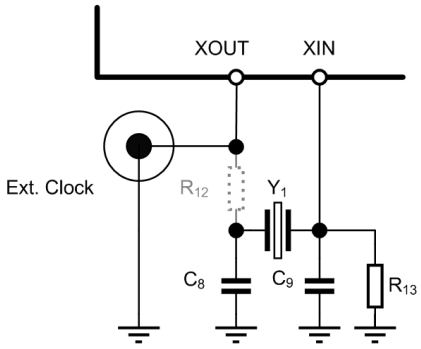

Figure 7. Clock Generation Circuit (External Clock)

UART Interface IDC_3

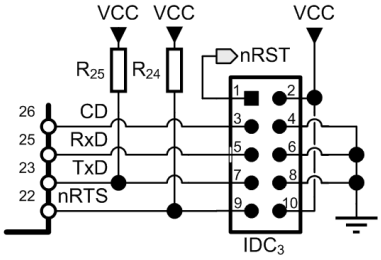

Figure 8. UART Interface (IDC_3)

Table 4. MICROCONTROLLER INTERFACE

Pin Number	Signal	Type	Description
1	RESETB	Open Drain	Reset Signal from the Voltage Supervisor, Open Drain with Pull-up, Active Low
3	CD	Output	Carrier Detect
5	RxD	Input	Receive from Microcontroller
7	TxD	Output	Transmit towards Microcontroller
9	RTSB	Input	Request to Send, Active Low
2, 10	VDD	Power	3 V Nominal
4, 6, 8	GND	Power	Ground

The interface towards a microcontroller is provided in IDC_3. This interface can also be used to supply power to the module. The nominal supply voltage for the module is 3 V. For more information see the section on power supply and references.

The RESETB line to the modem is an open drain signal. A pull-up resistor of 220 kΩ is provided on the board, and should not be duplicated on the microcontroller side. The reset signal is generated on the board, and could be used as reset signal for other IC such as the microcontroller.

The CD signal rises when a HART signal of ca. 100 mVpp is detected on the current loop. See the section on reference voltages for more information on these threshold level settings. When no signal, or a signal of limited amplitude is present, the CD line is pulled down to 0 V.

The RxD, TxD, and RTSB signals implement a standard UART interface at 1200 baud with start bit, 8 data bits, parity bit and stop bit (11-bit frame). The RTSB signal disconnects the transmitter circuit when pulled high, and should be held low before any data is transmitted. Data frames are not buffered by the modem. Instead, data is transmitted bit by bit. Care should be taken to avoid clock skew in the receiving UART. If the same time base is used for both the modem and the UART, a 1% accurate time base may not be sufficient. The problem is a combination of receive data jitter and clock skew between transmitting and receiving HART devices. If the transmit time base is at 99% of nominal and the receive time base in another device is at 101% of nominal, the receive data (at the receiving UART) will be skewed by roughly 21% of one bit time at the end of each 11-bit byte. This is shown in Figure 9. The skew time is measured from the initial falling edge of the start bit to the center of the 11th bit cell. This 21% skew by itself is a relatively good result. However, there is another error source for bit boundary jitter. The Phase Lock Loop demodulator in the NCN5193 produces jitter in the receive data that can be as large as 12% of a bit time. Therefore, a bit boundary can be shifted by as much as 24% of a bit time relative to its ideal location based on the start-bit transition. (The start-bit transition and a later transition can be shifted in opposite directions for a total of 24%).

The clock skew and jitter added together is 45%, which is the amount that a bit boundary could be shifted from its expected position. UARTs that sample at mid-bit will not be affected. However, there are UARTs that take multiple samples during each bit to try to improve on error performance. These UARTs may not be satisfactory, depending on how close the samples are to each other, and how samples are interpreted. A UART that takes a majority vote of 3 samples is acceptable.

Even if your own time base is perfect, you still must plan on a possible 35% shift in a bit boundary, since you don't have control over time bases in other HART devices.

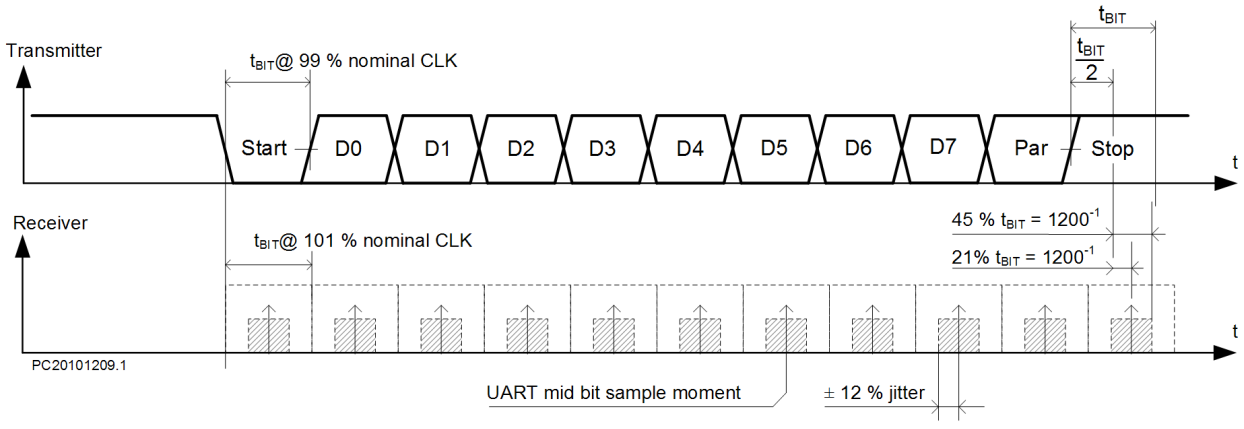

Figure 9. Clock Skew

SPI Interface and Internal Register

The NCN5193 also has an SPI interface that is used to control the integrated DAC and set the configuration registers of the IC. This interface is accessible on the evaluation board through connector IDC_1.

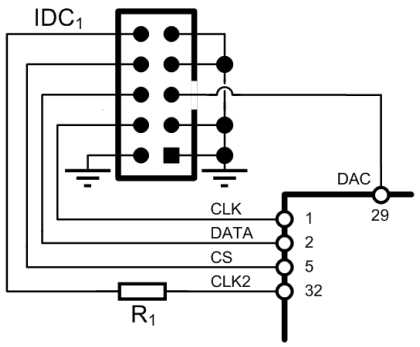

Figure 10. SPI Interface (IDC_1)

Table 5. SPI/DAC INTERFACE

Pin Number	Signal	Type	Description
5	DAC	Output	DAC Output
4	CLK	Input	SPI Clock
6	DATA	Input	SPI Data in (MOSI)
8	CS	Input	SPI Chip Select
1, 2, 3, 7, 9	GND	Power	
10	CLK2	Output	Clock Output 2

At reset of the device, all bits of the internal register are set to their reset value. This means that, before being able to use the evaluation board, the device must be configured and all required blocks must be turned on. See the description of the internal registers in the NCN5193 datasheet for more information.

Internal Sigma-Delta DAC

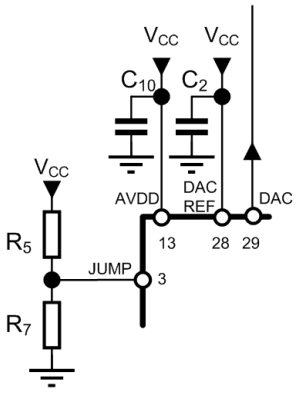

Figure 11. DAC Interface

The NCN5193 includes an internal DAC that can be used for the implementation of a slave analog transmitter.

The included DAC has a Sigma-Delta topology. This means that the output of the DAC is constantly switching between 0 V en DACREF (3 V on the evaluation board). To achieve optimum accuracy, it is required that DACREF is sufficiently decoupled from the power supply, such as by a large-value ceramic capacitor (1 μF typical).

The switching output signal will have the desired DC (low frequency) component, but also includes a lot of switching noise that needs to be filtered out before the signal is useful. This means that an output low pass filter is required before the DAC output can be used. Since the sigma-delta modulator is designed for a bandwidth of 25 Hz, it is advised that the corner frequency of the output filter is placed on this frequency.

For more information on how to design this filter, see the section on slave implementation.

To achieve maximum accuracy of the DAC, it is also advised to use a separate, low-noise reference as DACREF instead of tying this pin to V_{DD}, and to keep the DAC line away from noisy signal lines.

Transmitter

The TxA modem pin is accessible through pin 7 of IDC_2. For certain applications, it might be required to couple the transmit signal in the circuit by adding a series capacitor. Note that this is a difference with the A5191HRTNEVB, where this coupling capacitor was provided on the board. The output on this pin is a 500 mVpp signal trapezoid waveform shown in figure 11. This pin can only drive impedances higher than 30 kΩ, and as a consequence may need to be amplified.

The nominal frequency of the output is 1200 Hz for “mark” and 2200 Hz for “space”. These frequencies are dependent on the accuracy of the NCN5193 clock.

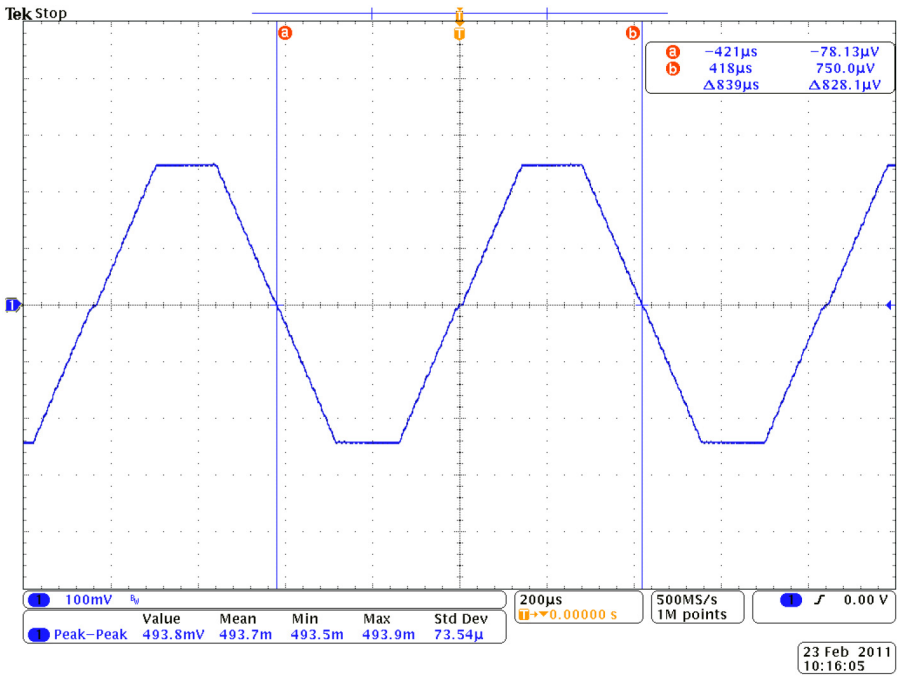

Figure 12. Output Waveform (Mark)

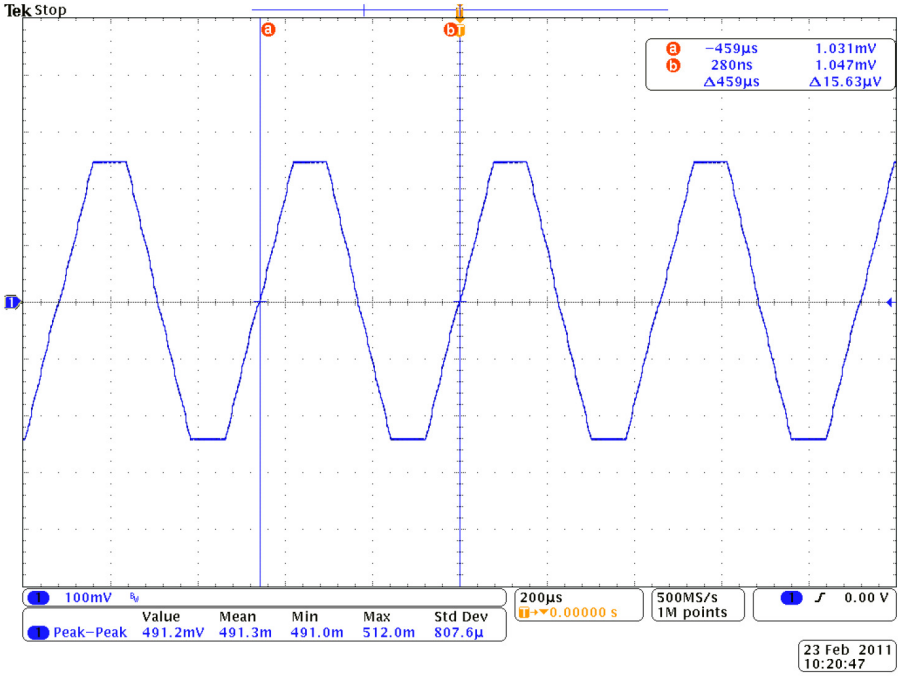

Figure 13. Output Waveform (Space)

Receiver

The receive band pass filter is implemented on the NCN5193NGEVB. The values are listed in Table 6 and the filter schematic is displayed in Figure 14. This is a band pass filter based on a Sallen-Key topology allowing only frequencies around the HART signal frequencies to pass through. For a more detailed description of the filter see the user manual of A5191HRTNEVB.

Table 6. RECEIVE FILTER COMPONENT VALUES

Reference	Value
R_{15}	2.2 MΩ, 1%
R_{16}	1.3 MΩ, 1%
R_{17}, R_{23}	422 kΩ, 1%
R_{18}, R_{22}	1.5 MΩ, 1%
R_{21}, R_{26}	806 kΩ, 1%
R_{27}	174 kΩ, 1%
C_7	1 nF, 5%
C_{11}	470 pF, 5%
C_{12}	20 pF, 5%
C_{13}	200 pF, 5%
C_{14}	220 pF, 5%
C_{15}	330 pF, 5%

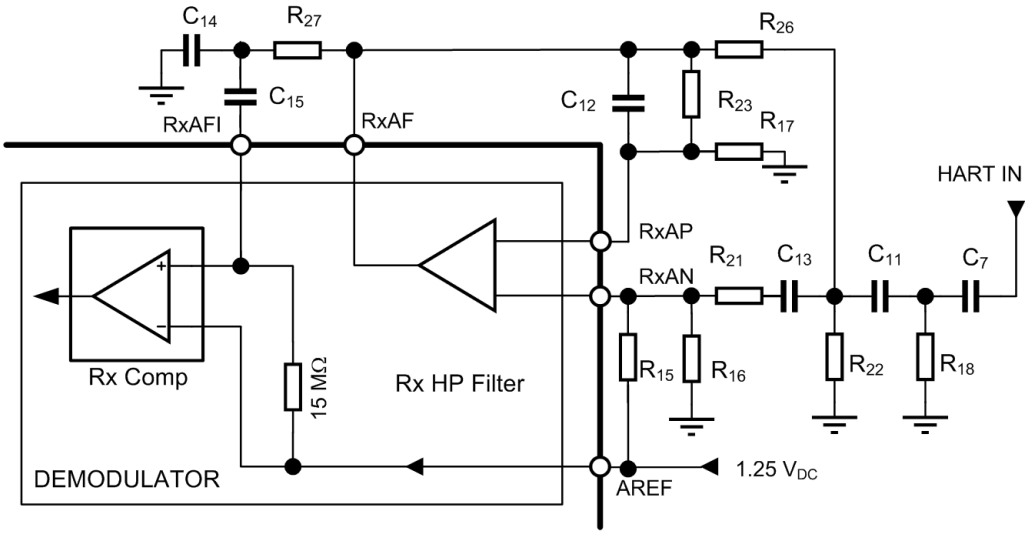

Figure 14. Receive Filter

APPLICATION IDEAS

The NCN5193 takes care of generating the HART modulation. This HART signal must then be superimposed on a 4−20 mA current loop. The NCN5193 simplifies slave implementation by including an integrated DAC. Below are some possible implementations of both a master and slave transmitter.

Slave Implementation

A simple slave implementation is shown in Figure 16. The analog loop current is set by the integrated DAC, and HART signals are added to this by a resistive summing network. The DAC is implemented as a sigma-delta modulator, which means that additional filtering should be implemented. To explain the operation of this circuit, let us first look at an example where the DAC is not of a switching topology, such as shown in Figure 15. As one end of R_6 is tied to local ground, and current passing through R_7 also passes through R_6, it can easily be seen that the voltage at the negative loop terminal is negative with respect to the local ground. Resistor R_4 is then chosen so that in steady state their common terminal is a virtual ground point in the absence of HART signals, since the negative terminal of the amplifier is also connected to ground. A similar principle applies when HART signals are applied. So both amplifier inputs are regulated to ground.

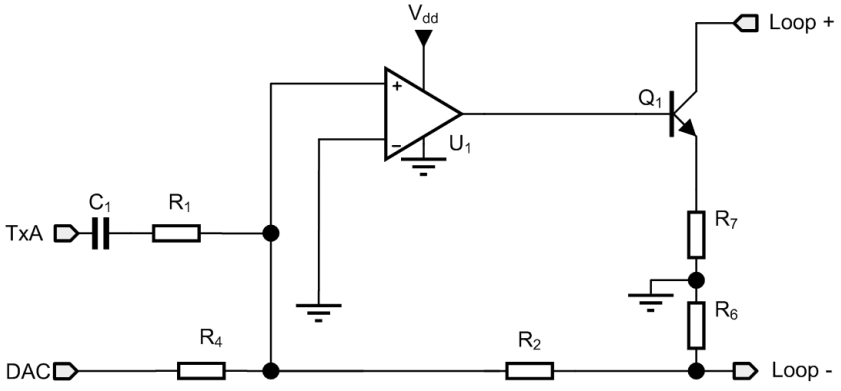

Figure 15. Simple Slave Implementation

A compensation capacitor C_4 may be required depending on the operational amplifier used. To avoid offset generated by bias current in the operational amplifier, a resistor R_3 should be placed on the negative input, and dimensioned to approach the impedance seen by the positive terminal.

The amplifier will then determine the current flowing through the loop by changing the base of a transistor in emitter feedback configuration. The value for R_7 is determined by the output range $V_{o,max}$ of the amplifier used:

$$R_{7,\,max} = \frac{V_{o,\,max} - V_{BE}}{20\ mA}$$

It is often recommended to take a value as large as possible, so that noise effects are minimal.

Typically the value of R_6 is chosen equal to R_7. The voltage over R_6 and R_7 combined should however be less than 12 V when the current setting is 20 mA.

Next, the value of R_4 is chosen depending on the most significant bit of the DAC.

$$2\ V_{MSB}\ R_2 = 20\ mA\ R_6\ R_4$$

When the DAC is not a switching topology, we can now choose R_1 and C_1. We have:

$$500\ mV\ R_2 = 1\ mA\ R_6\ Z$$

Where:

$$Z = \left|\frac{1}{sC_1} + R_1\right|$$

In practice, C_1 is chosen sufficiently large so that $Z \approx R_1$.

Because the integrated DAC has a sigma-delta output, a circuit using the NCN5193 gets a bit more complicated, as can be seen in Figure 16. We need to filter away high frequency DAC components, but leave HART signals intact. A simple RC-filter is not sufficient, since the output capacitor has low impedance for HART frequencies. We can do this by replacing the summing resistor R_4 by a T-filter. This filter has high output impedance due to the output resistor.

To dimension this filter without too much calculation, we can treat it as a RC-filter using its first branch. The 3-dB frequency should be placed just above the DAC bandwidth (10 Hz).

We get, with $R_4 \approx R_5$:

$$f_{3dB} = \frac{1}{2\pi\ C_3\ R_4}$$

To dimension the summing resistor of the HART input, we can no longer assume that the positive input of the amplifier is a virtual ground, as this assumption is only valid for DC signals. We can, however, find a relationship between input amplitude and output amplitude. We know that the positive amplifier input voltage has the following form, due to the summing network:

$$V_+ = \left(R_1//R_2//(R_4 + R_5)\right)\left(\frac{V_{in}}{R_1} - \frac{V_{out}}{R_2}\right)$$

The amplifier is configured as an integrator for low frequencies, but for high frequencies, the amplifier configuration has a gain of 1, and the transistor is configured as a voltage follower, so we can conclude that for AC frequencies $V_+ = V_{out}$. Taking this into account, we get the following equation:

$$V_{out} = \frac{R_2}{R_1}\frac{\left(R_1//R_2//(R_4 + R_5)\right)}{\left(R_1//R_2//(R_4 + R_5)\right) + R_2} V_{in}$$

Reconfiguring for the unknown R_1:

$$R_1 = \frac{R_2(R_4 + R_5)V_{in} + V_{out}(R_2 + R_3)}{V_{out}\left(1 + (R_4 + R_5)\right)}$$

The amplifier is configured as an integrator for low frequencies. Care must be taken that the 3-dB frequency of the integrator is below the HART band, so that the amplifier gain in that band is independent of frequency. The resistor R_3 is chosen so that it compensates for input bias current. This is achieved by taking a value close to the resistance seen on the positive terminal. This means that the capacitor C_2 needs to be chosen so that $(2\,\pi\,R_3C_2)^{-1} < 1$ kHz.

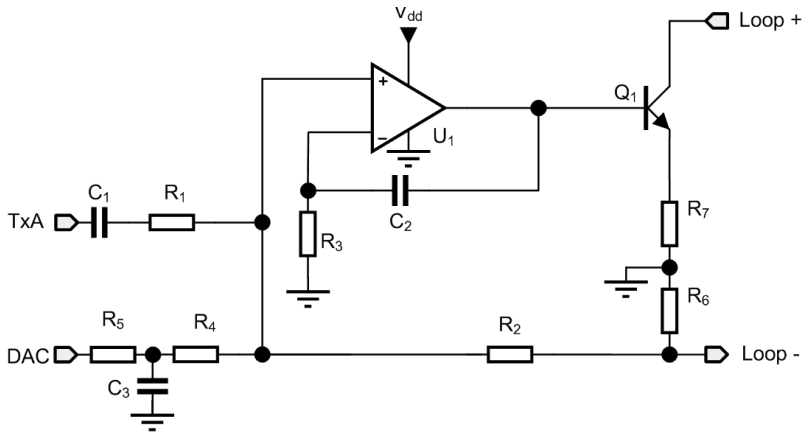

Figure 16. Sample Slave Implementation

Master Implementation

An example of a possible master implementation is shown in Figure 17.

The current loop master has a sense resistor over which the current flowing through the loop can be measured. The value of this resistor varies depending on the sensitivity required and range of the ADC. A HART Master can have a sense resistor ranging from 230 Ω to 600 Ω. Increasing the sense resistor will result in higher amplitude HART signal received, but will also reduce the voltage available on the slave side. Furthermore, if you wish to sense the analog transmitted signal, the MSB of your DAC may limit the resistor size. If this limitation is too stringent, the sense resistor can be split in two resistors, as shown in the figure, effectively creating a resistor divider.

To transmit a HART signal, the TxA signal will need to be amplified, as the NCN5193 transmit circuit can only drive high impedance circuits (> 30 kΩ). An additional operational amplifier is required. Depending on the sense resistor used, some gain or attenuation may be required to get a 1 mA peak-to-peak HART output signal. This can be accomplished by the resistors R_3 and R_4. For a typical sense resistor of 500 Ω, a unity gain suffices and a unity gain operational amplifier configuration can be used instead.

The amplifier however has a low impedance output, which cannot be paralleled with the sense resistor, as this would cause problems when the slave is transmitting. This problem is solved by adding a series switch (such as MC74VHC1G66DTT1G), controlled by the RTS signal. For a normally open switch, the nRTS signal as applied to the NCN5193 must be inverted first. To reduce power usage, the operational amplifier can be disabled when the transmitter is turned off. This is both done by inserting PNP transistor Q_1on the V_{DD} connection of the amplifier.

To couple the signal into the current loop, a single capacitor was used. For other coupling techniques see application note AND8346/D.

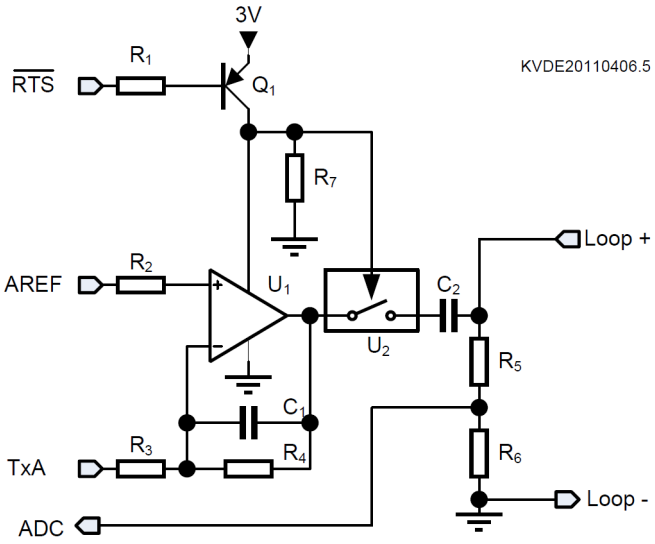

Figure 17. Sample Master Implementation

APPENDIX

Evaluation Board Layout

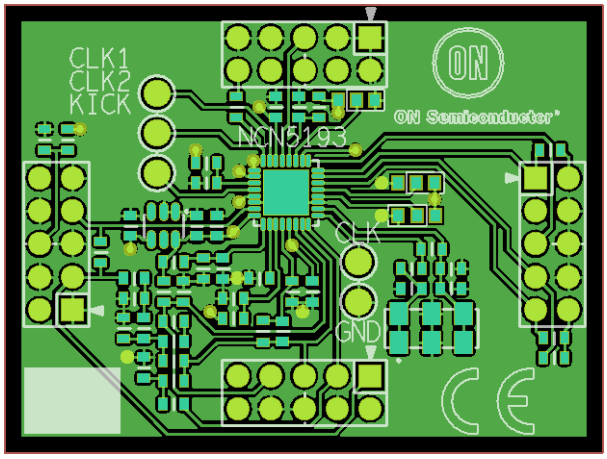

Figure 18. Top Layer Layout

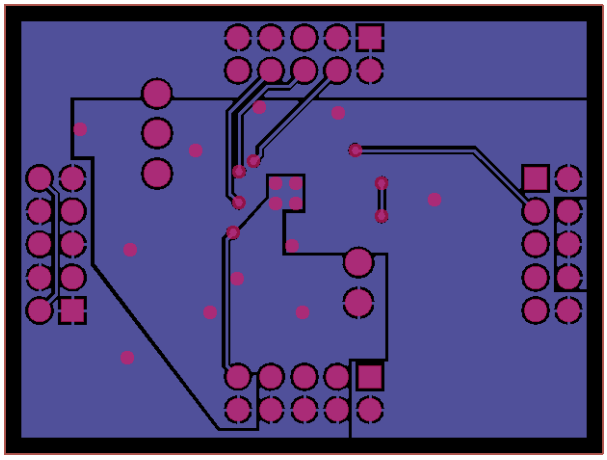

Figure 19. Bottom Layer Layout

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